AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Previously Presented) A level shifter comprising:

an inverter having an input node and an intermediate node, the input node having a logic state, the intermediate node having a logic state opposite of the logic state of the input node;

a first transistor that contacts the inverter and a first output node, the first output node having a logic state;

a second transistor that contacts the inverter and a second output node, the second output node having a logic state opposite the logic state of the first output node;

a third transistor that contacts the first transistor and the first output node;

a fourth transistor that contacts the second transistor and the second output node;

a fifth transistor that contacts the second transistor;

a sixth transistor that contacts the fifth transistor; and

a seventh transistor that contacts the fifth transistor, the sixth transistor, and the second output node.

3. (Original) The level shifter of claim 2 wherein the sixth transistor contacts the first output node.

4. (Previously Presented) The level shifter of claim 3 wherein the inverter is connected to receive a first supply voltage.

5. (Previously Presented) The level shifter of claim 4 wherein the first, second, fifth, and seventh transistors are connected to receive ground, and the third, fourth, and sixth transistors are connected to receive a second supply voltage, the second supply voltage being greater than the first supply voltage.

6. (Original) The level shifter of claim 3 wherein the fifth and sixth transistors are MOS transistors, and the seventh transistor is a bipolar transistor.

7. (Original) The level shifter of claim 3 wherein the third transistor has a gate and a drain, and the fourth transistor has a gate that contacts the drain of the third transistor, and a drain that contacts the gate of the third transistor.

8. (Previously Presented) The level shifter of claim 2 and further comprising:

an eighth transistor that contacts the first transistor;

a ninth transistor that contacts the eighth transistor; and

a tenth transistor that contacts the eighth transistor, the ninth transistor, and the first output node.

9. (Original) The level shifter of claim 8 wherein the ninth transistor contacts the second output node.

10. (Previously Presented) The level shifter of claim 9 wherein the inverter is connected to receive a first supply voltage.

11. (Previously Presented) The level shifter of claim 10 wherein the first, second, fifth, seventh, eighth, and tenth transistors are connected to receive ground, and the third, fourth, sixth, and ninth transistors are connected to receive a second supply voltage, the second supply voltage being greater than the first supply voltage.

12. (Original) The level shifter of claim 9 wherein the fifth and sixth transistors are MOS transistors, and the seventh transistor is a bipolar transistor.

13. (Previously Presented) The level shifter of claim 2 wherein the inverter is connected to a first supply voltage, and the third and fourth transistors are connected to a second supply voltage, the second supply voltage being greater than the first supply voltage.

14. (Previously Presented) A method of level shifting a voltage, the method comprising pulling down an intermediate voltage on a first intermediate node to a first value when an input voltage on an input node has a logic high, the first value turning off a first transistor and a second transistor, the logic high turning on a third transistor and a fourth transistor, the third transistor pulling down an output voltage on an inverting output node, the fourth transistor pulling down an intermediate voltage on a second intermediate node to a second value, the second value turning on a fifth transistor that pulls down the output voltage on the inverting output node.

15. (Previously Presented) The method of claim 14 and further comprising pulling up the intermediate voltage on the first intermediate node to a third value when an input voltage on the input node has a logic low, the third value turning on the first transistor and the second transistor, the logic low turning off the third transistor and the fourth transistor, the first transistor pulling down an output voltage on a non-inverting output node, the second transistor pulling down an intermediate voltage on a third intermediate node to a fourth value, the fourth value turning on a sixth transistor that pulls down the output voltage on the non-inverting output node.

16. (Previously Presented) A level shifter comprising:

a level shifting circuit having an input, an inverted output, and a non-inverted output, a logic high at the input having a first voltage, a logic high at the inverted output having a second voltage, a logic high at the non-inverted output having the second voltage, the second voltage being greater than the first voltage; and

a pull down circuit connected to the level shifting circuit that sinks current from the inverted output when the level shifting circuit sinks current from the inverted output, and from the non-inverted output when the level shifting circuit sinks current from the non-inverted output.

17. (Previously Presented) The level shifter of claim 16 wherein the pull down circuit includes:

a first transistor connected between the inverted output and ground; and

a second transistor isolated from the inverted output, the second transistor being connected to the first transistor and the level shifting circuit to turn on the first transistor when the level shifting circuit sinks current from the inverted output.

18. (Previously Presented) The level shifter of claim 17 wherein the level shifting circuit includes a pull down transistor that sinks current from the inverted output when pulling down a voltage on the inverted output to ground, the second transistor being connected to the pull down transistor.

19. (Currently Amended) ~~The level shifter of claim 17 wherein the pull down circuit includes:~~ A level shifter comprising:

a level shifting circuit having an input, an inverted output, and a non-inverted output, a logic high at the input having a first voltage, a logic high at the inverted output having a second voltage, a logic high at the non-inverted output having the second voltage, the second voltage being greater than the first voltage; and

a pull down circuit connected to the level shifting circuit that sinks current from the inverted output when the level shifting circuit sinks current from the inverted output, and from the non-inverted output when the level shifting circuit sinks current from the non-inverted output, the pull down circuit including:

a first transistor connected between the inverted output and ground; and

a second transistor isolated from the inverted output, the second transistor being connected to the first transistor and the level shifting circuit to turn on the first transistor when the level shifting circuit sinks current from the inverted output;

a third transistor connected between the non-inverted output and ground; and

a fourth transistor isolated from the non-inverted output, the fourth transistor being connected to the third transistor and the level shifting circuit to turn on the third transistor when the level shifting circuit sinks current from the non-inverted output.

20. (Previously Presented) The level shifter of claim 19 wherein the level shifting circuit includes:

a first pull down transistor that sinks current from the inverted output when pulling down a voltage on the inverted output to ground, the second transistor being connected to the first pull down transistor; and

a second pull down transistor that sinks current from the non-inverted output when pulling down a voltage on the non-inverted output to ground, the fourth transistor being connected to the second pull down transistor.

21. (Previously Presented) The level shifter of claim 19 and further comprising:

a first PMOS transistor connected to the non-inverted output and the second transistor; and

a second PMOS transistor connected to the inverted output and the fourth transistor.